OMAP35x Peripherals Overview

Texas Instruments OMAP™ Family of Products

Reference Guide

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About This Manual

This document provides an overview and briefly describes the peripherals available on the OMAP35x Applications Processor.

Related Documentation From Texas Instruments

The following documents describe the OMAP35x Applications Processor. The OMAP35x Applications Processor, related peripherals, and other technical collateral, is available in the OMAP DSP product folder at: www.ti.com/omap.

SPRUF98 — *OMAP35x Technical Reference Manual.* Collection of documents providing detailed information on the OMAP3 architecture including power, reset, and clock control, interrupts, memory map, and switch fabric interconnect. Detailed information on the microprocessor unit (MPU) subsystem, the image, video, and audio (IVA2.2) subsystem, as well a functional description of the peripherals supported on OMAP35x devices is also included.

SPRU732 — *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide.* Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C64x and TMS320C64x+ digital signal processors (DSPs) of the TMS320C6000 DSP family. The C64x/C64x+ DSP generation comprises fixed-point devices in the C6000 DSP platform. The C64x+ DSP is an enhancement of the C64x DSP with added functionality and an expanded instruction set.

SPRU871 — *TMS320C64x+ DSP Megamodule Reference Guide.* Describes the TMS320C64x+ digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

SPRU889 — *High-Speed DSP Systems Design Reference Guide.* Provides recommendations for meeting the many challenges of high-speed DSP system design. These recommendations include information about DSP audio, video, and communications systems for the C5000 and C6000 DSP platforms.

Trademarks

OMAP35x Peripherals Overview

1 Overview

This document provides an overview and briefly describes the peripherals available on the OMAP35x Applications Processor.

The OMAP35x Technical Reference Manual (literature number SPRUF98) describes all peripherals in detail and provides additional information about the OMAP35x applications processors. Table 1 provides a list of the information contained in the chapters of the OMAP35x Technical Reference Manual.

The OMAP35x Technical Reference Manual can be downloaded as a single document or it can be downloaded on a chapter-by-chapter basis by using the literature numbers given in Table 1.

The sections that follow provide an overview of the peripherals and other modules available in the OMAP35x applications processors.

Note: Some features may not be available or supported in your particular device. For more information, see Chapter 1, the *OMAP35x Family* section, and your device-specific data manual.

Table 1. Breakdown of OMAP35x Technical Reference Manual

Peripheral/Module/Other	Acronym	Chapter	Lit #
Introduction		Chapter 1	SPRUFF1
Memory Mapping		Chapter 2	SPRUFF2
Microprocessor Unit Subsystem	MPU	Chapter 3	SPRUFA0
Power, Reset, and Clock Management	PRCM	Chapter 4	SPRUFA5
Interconnect		Chapter 5	SPRUFF3
Interprocessor Communication Module	IPC	Chapter 6	SPRUFF4
System Control Module	SCM	Chapter 7	SPRUFA6
Memory Management Units	MMU	Chapter 8	SPRUFF5
System Direct Memory Access	SDMA	Chapter 9	SPRUFA7
Interrupt Controller	INTC	Chapter 10	SPRUFA8
Memory Subsystem - General-Purpose Memory Controller	GPMC	Chapter 11	SPRUFA1
Memory Subsystem - SDRAM Controller Subsystem	SDRC	Chapter 11	SPRUFA1
Memory Subsystem - On-Chip Memory Subsystem	OCM	Chapter 11	SPRUFA1
Camera Interface Subsystem	ISP	Chapter 12	SPRUFA2
2D/3D Graphics Accelerator	SGX	Chapter 13	SPRUFF6
Image Video and Audio Accelerator Subsystem	IVA2.2	Chapter 14	SPRUFA3
Display Interface Subsystem		Chapter 15	SPRUFA4
Timers		Chapter 16	SPRUFA9
Universal Asynchronous Receiver/Transmitter Module	UART	Chapter 17	SPRUFC5
Infrared Data Association Module	IrDA	Chapter 17	SPRUFC5
Consumer Infrared Module	CIR	Chapter 17	SPRUFC5
Inter-Integrated Circuit Module	I^2C	Chapter 18	SPRUFC6

Table 1. Breakdown of OMAP35x Technical Reference Manual (continued)

Peripheral/Module/Other	Acronym	Chapter	Lit #
Multi-channel Serial Port Interface	McSPI	Chapter 19	SPRUFC9
HDQ/1-Wire Module		Chapter 20	SPRUFD0
Multi-Channel Buffered Serial Port	McBSP	Chapter 21	SPRUFD1
Multimedia Card/Secure Digital/ Secure Digital I/O Card Interface	MMC/SD/SDIO	Chapter 22	SPRUFD2
High-Speed Universal Serial Bus (USB) OTG Controller and High-Speed USB Host Subsystem	USB	Chapter 23	SPRUFD4
General-Purpose I/O Interface	GPIO	Chapter 24	SPRUFD5
Applications Processor Initialization		Chapter 25	SPRUFD6

2 Memory Management Units (MMU)

The OMAP35x device contains three memory management units (MMU):

- Microprocessor unit (MPU) MMU.
- Camera MMU.
- Image Video and Audio accelerator (IVA2.2) MMU.

The camera MMU and IVA2.2 MMU share the same architecture and are both described in this chapter. The MPU MMU, which implements a different architecture, is covered in the *ARM® CORTEX™-A8 Technical Reference Manual*.

Note: The MMUn prefix provides information about the register instantiation, where n = 1 for the camera MMU, and n = 2 for the IVA2.2 MMU.

The MMU instances include the following main features:

- N entries fully associative translation look-aside buffer (TLB) with N = 8 for the camera MMU and N = 32 for the IVA2.2 MMU.
- 1 interrupt line out to the MPU subsystem.
- 32-bit virtual addresses, 32-bit physical address.
- Mapping size: 4KB and 64KB pages, 1MB section, and 16MB supersection.
- Predefined (static) or table-driven (hardware table walker) software translation strategies.

For more information about the memory management units, please refer to the *Memory Management Units (MMU)* chapter of the OMAP35x Technical Reference Manual.

3 System Direct Memory Access (SDMA)

The System Direct Memory Access (SDMA), also called DMA4, performs high-performance data transfers between memories and peripheral devices without microprocessor unit (MPU) support during transfer. A DMA transfer is programmed through a logical DMA channel, which allows the transfer to be optimally tailored to the requirements of the application.

The DMA controller includes the following main features:

- Data transfer support in either direction between:
  - Memory and memory
  - Memory and peripheral device
- 32 logical DMA channels supporting:
  - Multiple concurrent transfers
  - Independent transfer profile for each channel
  - 8-bit, 16-bit, or 32-bit data element transfer size
  - Software-triggered or hardware-synchronized transfers

  - Flexible source and destination address generation
  - Burst read and write
  - Chained multiple-channel transfers
  - Endianism conversion
  - Per-channel secure transaction attribute (not available on GP device)
- First-come, first-serve DMA scheduling with fixed priority
- Up to 96 DMA requests
- Constant fill
- Transparent copy
- Four programmable interrupt request output lines
- Software or hardware enabling
- FIFO depth: 256 x 32-bits
- Data buffering
- FIFO budget allocation
- Power-management support
- Auto-idle power-saving support
- Implementation of retention flip-flops (RFFs) to support dynamic power saving (DPS) between system power modes without MPU involvement
- Initiators for secure transactions on the L3 and L4 interconnect (not available on GP device)

The SDMA module has two ports—one read and one write—and provides multiple logical channel support. A dynamically allocated FIFO queue memory pool provides buffering between the read and write ports.

For more information about the system DMA, please refer to the *System Direct Memory Access (SDMA)* chapter of the OMAP35x Technical Reference Manual.

4 General-Purpose Memory Controller (GPMC)

The general-purpose memory controller (GPMC) is dedicated to interfacing external memory devices:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous, and page mode (only available in non-muxed mode) burst NOR flash devices
- NAND flash
- Pseudo-SRAM devices

For more information about the GPMC, please refer to the *Memory Subsystem* chapter of the OMAP35x Technical Reference Manual.

5 SDRAM Controller Subsystem (SDRC)

The SDRC subsystem module provides connectivity between the OMAP Applications Processor and external discrete or POP-ed low-power double-data-rate SDRAM (LPDDR).

The SDRC subsystem provides a high-performance interface to a variety of fast memory devices. It comprises two submodules:

- The SDRAM Memory Scheduler (SMS), consisting of scheduler, security firewall, and virtual rotated frame-buffer (VRFB) modules.
- The SDRAM Controller.

For more information about the SDRC, please refer to the *Memory Subsystem* chapter of the OMAP35x Technical Reference Manual.

6 Camera Interface Subsystem (ISP)

The camera ISP is a key component for imaging and video applications such as video preview, video record, and still-image capture with or without digital zooming.

The camera ISP provides the system interface and the processing capability to connect RAW image-sensor modules to the OMAP35x Applications Processor.

The camera ISP can support the following features:

- Image sensor.
- Parallel interface: The parallel interface supports two modes.
- Video processing: The video-processing hardware removes the need for expensive camera modules to perform processing functions. The video-processing hardware contains a real-time image-pipeline and resizer.
- Statistic collection modules (SCM): The host CPU uses statistics to adjust various parameters for processing image data. The SCM provides statistics in real-time.
- Central-resource shared buffer logic (SBL): Buffers and schedules memory accesses requested by camera ISP modules.
- Circular buffer: Prevents storage of full image frames in memory when data must be postprocessed and/or preprocessed by software.
- Memory management unit (MMU): Manages virtual-to-physical address translation for external addresses and solves the memory-fragmentation issue. Enables the camera driver to dynamically allocate and deallocate memory; the MMU handles memory fragmentation.
- Clock generator: Generates two independent clocks that can be used by two external image sensors.
- Secure mode: Used to store sensitive captured images.
- Timing control.
- Open core protocol (OCP) compliant.

For more information about the camera ISP, please refer to the *Camera Interface Subsystem (ISP)* chapter of the OMAP35x Technical Reference Manual.

7 2D/3D Graphics Accelerator (SGX)

The 2D/3D graphics accelerator subsystem accelerates 2-dimensional (2D) and 3-dimensional (3D) graphics applications. The SGX subsystem is based on the SGX core from Imagination Technologies. SGX is a new generation of programmable PowerVR graphics and video IP cores. The PowerVR SGX architecture is scalable and can target all market segments from mainstream mobile devices to high-end desktop graphics. Targeted applications include feature phone, PDA, and hand-held games.

The SGX graphics accelerator efficiently processes a number of various multimedia data types concurrently:

- Pixel data
- Vertex data
- Video data
- General-purpose processing

This is achieved using a multithreaded architecture using two levels of scheduling and data partitioning enabling zero overhead task switching.

For more information about the 2D/3D graphics accelerators, please refer to the *2D/3D Graphics Accelerator (SGX)* chapter of the OMAP35x Technical Reference Manual.

8 Image Video and Audio Accelerator Subsystem (IVA2.2)

The image video and audio accelerator (IVA2.2) is based on the TMS320DMC64X+ VLIW digital signal processor (DSP) core.

The internal architecture is an assembly of the following components:

- High-performance TI DSP (TMS320DMC64X+) integrated in a megacell, including local L1/L2 cache and memory controllers
- L1 RAM and L2 RAM and ROM
- Video hardware accelerator
- Dedicated enhanced data memory access (EDMA) engine to download/upload data from/to memories and peripherals external to the sub-chip
- Dedicated memory management unit (MMU) for accessing level 3 (L3) interconnect address space
- Local interconnect network
- Dedicated modules SYSC and WUGEN in charge of power management, clock generation, and connection to the power, reset, and clock manager (PRCM) module

For more information about the IVA2.2 subsystem, please refer to the *Image Video and Audio Accelerator Subsystem (IVA2.2)* chapter of the OMAP35x Technical Reference Manual.

9 Display Interface Subsystem

The display interface subsystem provides the logic to display a video frame from the memory frame buffer (either SDRAM or SRAM) on a liquid-crystal display (LCD) panel or a TV set. The display subsystem integrates the following elements:

- Display controller (DISPC) module
- Remote frame buffer interface (RFBI) module
- NTSC/PAL video encoder

For more information about the display interface subsystem, please refer to the *Display Interface Subsystem* chapter of the OMAP35x Technical Reference Manual.

10 Timers

The device has 12 GP timers: GPTIMER1 through GPTIMER12.

Each timer can be clocked from either the system clock (12, 13, 16.8, 19.2, 26, or 38.4 MHz) or the 32-kHz clock. The selection of the clock source is made at the power, reset, clock management (PRCM) module level.

GPTIMER1 has its GPT1_EVENT_CAPTURE pin tied to the 32-kHz clock and can be used to gauge the system clock input; it detects its frequency among 12, 13, 16.38, 19.2, 26, or 38.4 MHz.

Each timer can provide an interrupt to the microprocessor unit (MPU) subsystem. In addition, GPTIMER5 through GPTIMER8 also have interrupts connected to the IVA2.2 subsystem.

GPTIMER1, GPTIMER2, and GPTIMER10 include specific functions to generate accurate tick interrupts to the operating system. GPTIMER8 through GPTIMER11 are connected to external pins by their PWM output or their event capture input pin (for external timer triggering).

The following are the main features of the GP timers controllers:

- L4 slave interface support:
  - 32-bit data bus width
  - 32-/16-bit access supported
  - 8-bit access not supported
  - 10-bit address bus width
  - Burst mode not supported
  - Write nonposted transaction mode supported
- Interrupts generated on overflow, compare, and capture
- Free-running 32-bit upward counter
- Compare and capture modes
- Autoreload mode
- Start/stop mode
- Programmable divider clock source (2^n with n = [0:8])

- Dedicated input trigger for capture mode and dedicated output trigger/PWM signal
- Dedicated output signal for general-purpose using GPTi_GPOCFG signal
- On-the-fly read/write register (while counting)
- 1-ms tick with 32,768 Hz functional clock generated (only GPTIMER1, GPTIMER2, and GPTIMER10)

For more information about the timers, please refer to the *Timers* chapter of the OMAP35x Technical Reference Manual.

11 Universal Asynchronous Receiver/Transmitter Module (UART)

The OMAP35x Applications Processor contains three universal asynchronous receiver/transmitter (UART) devices controlled by the microprocessor unit (MPU).

- Two UART-only modules, UART1 and UART2, are pinned out for use as UART devices only.

  UART1 and UART2 must be programmed by setting the UARTi.MDR1_REG[2:0] MODE_SELECT field to one of the three UART operating modes.
- UART3, which adds infrared communication support, is pinned out for use as a UART, infrared data association (IrDA), or consumer infrared (CIR) device, and can be programmed to any available operating mode.

The UARTs (UART1, UART2, and UART3 when in UART mode) include the following key features:

- 16C750 compatibility
- 64-byte FIFO for receiver and 64-byte FIFO for transmitter
- Programmable interrupt trigger levels for FIFOs
- Baud generation based on programmable divisors N (N = 1…16,384) operating from a fixed functional clock of 48 MHz

Oversampling is programmed by software as 16 or 13; thus, the baud rate computation is either:

- Baud rate = (functional clock/16)/N
- Baud rate = (functional clock/13)/N

This software programming mode enables higher baud rates with the same error amount without changing the clock source:

- Break character detection and generation
- Configurable data format
  - Data bit: 5, 6, 7, or 8 bits
  - Parity bit: Even, odd, none
  - Stop-bit: 1, 1.5, 2 bit(s)
- Flow control: Hardware (RTS/CTS) or software (XON/XOFF)

The UART clocks are connected to produce a baud rate of up to 3.6M bits/s.

For more information about the UARTs, please refer to the *Universal Asynchronous Receiver/Transmitter Module (UART)* chapter of the OMAP35x Technical Reference Manual.

12 Infrared Data Association Module (IrDA)

The IrDA (UART3 only) includes the following key features:

- Support of IrDA 1.4 slow infrared (SIR), medium infrared (MIR), and fast infrared (FIR) communications
  - Frame formatting: Addition of variable beginning-of-frame (xBOF) characters and end-of-frame (EOF) characters
  - Uplink/downlink cyclic redundancy check (CRC) generation/detection
  - Asynchronous transparency (automatic insertion of break character)
  - Eight-entry status FIFO (with selectable trigger levels) to monitor frame length and frame errors
  - Framing error, CRC error, illegal symbol (FIR), and abort pattern (SIR, MIR) detection

For more information about the IrDA, please refer to the *Infrared Data Association Module (IrDA)* chapter of the OMAP35x Technical Reference Manual.

13 Consumer Infrared Module (CIR)

The CIR mode uses a variable pulse-width modulation (PWM) technique (based on multiples of a programmable *t* period) to encompass the various formats of infrared encoding for remote-control applications. The CIR logic transmits and receives data packets based on a user-definable frame structure and packet content.

The CIR (UART3 only) includes the following key features to provide CIR support for remote control applications:

- Transmit and receive
- Free data format (supports any remote-control private standards)
- Selectable bit rate
- Configurable carrier frequency
- 1/2, 5/12, 1/3, or 1/4 carrier duty cycle

For more information about the CIR, please refer to the *Consumer Infrared Module (CIR)* chapter of the OMAP35x Technical Reference Manual.

14 Inter-Integrated Circuit Module (I^2C)

The OMAP35x Applications Processor contains three multimaster high-speed (HS) inter-integrated circuit (I^2C) controllers (I2Ci modules, where I = 1, 2, 3), each of which provides an interface between a local host (LH), such as the MPU subsystem, and any I^2C-bus-compatible device that connects through the I^2C serial bus. External components attached to the I^2C bus can serially transmit/receive up to 8 bits of data to/from the LH device through the 2-wire I^2C interface.

Each multimaster HS I^2C controller can be configured to act like a slave or master I^2C-compatible device. Moreover, each multimaster HS I^2C controller can be configured in serial camera control bus (SCCB) mode (the SCCB is a serial bus developed by Omnivision Technologies, Inc.) to act as a master on a 2-wire SCCB bus. Only multimaster HS I^2C controllers I2C2 and I2C3 can be configured in SCCB mode to act as a master device on a 3-wire SCCB bus.

The device contains an additional master transmitter HS I^2C interface (I2C4) in the PRCM module to perform dynamic voltage control and power sequencing. Texas Instruments Inc. provides a global solution with the device connected to power chips (TPS65950 device). For details about the TPS65950 device, contact your TI representative.

The three multimaster HS I^2C controllers have the following features:

- Compliance with Philips I^2C specification version 2.1
- Support for standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Support for HS mode for transfer up to 3.4M bits/s
- Support for 3-wire/2-wire SCCB master mode for I2C2 and I2C3 modules, 2-wire SCCB master mode for I2C1 module, up to 100K bits/s
- 7-bit and 10-bit device addressing modes
- General call
- Start/restart/stop
- Multimaster transmitter/slave receiver mode
- Multimaster receiver/slave transmitter mode
- Combined master transmit/receive and receive/transmit mode
- Built-in FIFO for buffered read or write
  - 8 bytes for I2C1 and I2C2
  - 64 bytes for I2C3
- Module enable/disable capability
- Programmable clock generation
- 8-bit-wide data access
- Low-power consumption design
- Two DMA channels

- Wide interrupt capability

The master transmitter HS I^2C controller I2C4 has the following features:

- Support of HS and fast modes
- 7-bit addressing mode only
- Master transmitter mode only
- Start/restart/stop

For more information about the I^2C, please refer to the *Inter-Integrated Circuit Module (I^2C)* chapter of the OMAP35x Technical Reference Manual.

15 Multi-channel Serial Port Interface (McSPI)

The multichannel serial port interface (McSPI) is a master/slave synchronous serial bus. There are four separate McSPI modules (SPI1, SPI2, SPI3, and SPI4) in the device. The McSPI modules differ as follows: SPI1 supports up to four peripherals, SPI2 and SPI3 support up to two peripherals, and SPI4 supports only one peripheral.

The McSPI instances include the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths ranging from 4 bits to 32 bits
- Up to four master channels or single channel in slave mode
- Master multichannel mode:
  - Full duplex/half duplex
  - Transmit-only/receive-only/transmit-and-receive modes
  - Flexible I/O port controls per channel
  - Two direct memory access (DMA) requests (read/write) per channel
- Single interrupt line for multiple interrupt source events
- Power management through wake-up capabilities
- Enable the addition of a programmable start-bit for SPI transfer per channel (start-bit mode)
- Support start-bit write command
- Support start-bit pause and break sequence
- 64 bytes built-in FIFO available for a single channel

For more information about the McSPI, please refer to the *Multi-channel Serial Port Interface (McSPI)* chapter of the OMAP35x Technical Reference Manual.

16 HDQ/1-Wire Module

The HDQ/1-Wire module implements the hardware protocol of the master functions of the Benchmark HDQ and the Dallas Semiconductor 1-Wire® protocols. These protocols use a single wire for communication between the master (HDQ/1-Wire controller) and the slave (HDQ/1-Wire external compliant device).

The HDQ and 1-Wire module has a generic L4 interface and is intended to be used in an interrupt-driven fashion. The one-pin interface is implemented as an open-drain output at the device level.

The HDQ operates from a fixed 12-MHz functional clock provided by the PRCM module.

Only the MPU subsystem uses the HDQ/1-Wire module.

The main features of the HDQ/1-Wire module support the following:

- Benchmark HDQ protocol
- Dallas Semiconductor 1-Wire® protocol
- Power-down mode

For more information about the HDQ/1-wire module, please refer to the *HDQ/1-Wire Module* chapter of the OMAP35x Technical Reference Manual.

17 Multi-Channel Buffered Serial Port (McBSP)

The multi-channel buffered serial port (McBSP) provides a full-duplex direct serial interface between the device and other devices in a system such as other application chips (digital base band), audio and voice codec (TPS65950 device), etc. Because of its high level of versatility, it can accommodate a wide range of peripherals and clocked frame oriented protocols.

The OMAP35x device provides five instances of the McBSP modules, called McBSP1, McBSP2, McBSP3, McBSP4,and McBSP5.

The main features of the McBSP modules are:

- L4 interconnect slave interface supports:
  - 32-bit data bus width
  - 32-bit access supported
  - 16- /8-bit access not supported
  - 10-bit address bus width
  - Burst mode not supported
  - Write nonposted transaction mode supported
- 128 x 32-bit words (512 bytes) for each buffer for transmit/receive operations (McBSP1, 3, 4, 5)
- 5K bytes (1024 x 32 bits for audio buffer + 256 $\times$ 32 bits for buffer) for each buffer for transmit/receive audio operations (McBSP2 only)
- Interrupts configurable in legacy mode (2 requests) or PRCM compliant (1 request)
- Transmit and receive DMA requests triggered with programmable FIFO thresholds
- SIDETONE core support: Audio loopback capability (McBSP2 and 3 only)
- Multidrop support
- Serial interface description
  - 6 pin configuration (McBSP 1 only)
  - 4 pin configuration (McBSP2, 3, 4, 5)
  - Full-duplex communication
  - Multichannel selection modes
    - Support to enable or block transfers in each of the channels
    - 128 channels for transmission and for reception
  - Direct interface to industry-standard codecs, analog interface chips (AICs), and other serially connected A/D and D/A devices:
    - Inter-IC sound (I2S) compliant devices
    - Pulse code modulation (PCM) devices
    - Time division multiplexed (TDM) bus devices
  - A wide selection of data sizes: 8, 12, 16, 20, 24, and 32 bits
  - Bit reordering (send/receive least significant bit [LSB])
- Clock and frame-synchronization generation support:
  - Independent clocking and framing for reception and for transmission up to 48 MHz
  - Support for external generation of clock signals and frame-synchronization (frame-sync) signals
  - A programmable sample rate generator for internal generation and control of clock signals and frame-sync signals
  - Programmable polarity for frame-sync pulses and for clock signals

For more information about the McBSP, please refer to the *Multi-Channel Buffered Serial Port (McBSP)* chapter of the OMAP35x Technical Reference Manual.

18 Multimedia Card/Secure Digital/Secure Digital I/O Card Interface (MMC/SD/SDIO)

The OMAP35x Applications Processor contains three multimedia card high-speed/secure data/secure digital I/O (MMC/SD/SDIO) host controller which provides an interface between a local host (LH) such as a microprocessor unit (MPU) or digital signal processor (DSP) and either MMC, SD memory cards, or SDIO cards and handles MMC/SD/SDIO transactions with minimal LH intervention.

The application interface manages transaction semantics. The MMC/SD/SDIO host controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRC), start/end bit, and checking for syntactical correctness.

The application interface can send every MMC/SD/SDIO command and either poll for the status of the adapter or wait for an interrupt request, which is sent back in case of exceptions or to warn of end of operation.

The application interface can read card responses or flag registers. It can also mask individual interrupt sources. All these operations can be performed by reading and writing control registers. The MMC/SD/SDIO host controller also supports two DMA channels.

The main features of the MMC/SD/SDIO host controller are:

- Full compliance with MMC command/response sets as defined in the *Multimedia Card System Specification*, v4.2. Including high-capacity (size >2GB) cards HC MMC.
- Full compliance with SD command/response sets as defined in the *SD Memory Card Specifications*, v2.0. Including high-capacity (size >2GB) cards HC SD.
- Full compliance with SDIO command/response sets and interrupt/read-wait mode as defined in the *SDIO Card Specification, Part E1*, v1.10
- Compliance with sets as defined in the *SD Card Specification, Part A2, SD Host Controller Standard Specification*, v1.00
- Full compliance with MMC bus testing procedure as defined in the *Multimedia Card System Specification*, v4.2
- Full compliance with CE-ATA command/response sets as defined in the *CE-ATA Standard Specification*
- Full compliance with ATA for MMCA specification
- Flexible architecture allowing support for new command structure
- Support:
  - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards
  - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards
- Built-in 1024-byte buffer for read or write
- 32-bit-wide access bus to maximize bus throughput
- Single interrupt line for multiple interrupt source events
- Two slave DMA channels (1 for TX, 1 for RX)
- Designed for low power
- Programmable clock generation
- Support SDIO Read Wait and Suspend/Resume functions
- Support Stop at block gap
- Support command completion signal (CCS) and command completion signal disable (CCSD) management as specified in the *CE-ATA Standard Specification*

For more information about the MMC/SD/SDIO ports, please refer to the *Multimedia Card/Secure Digital/Secure Digital I/O Card Interface (MMC/SD/SDIO)* chapter of the OMAP35x Technical Reference Manual.

19 High-Speed Universal Serial Bus (USB) OTG Controller and High-Speed USB Host Subsystem

The OMAP35x device includes a high-speed universal serial bus (USB) OTG controller and a high-speed USB host subsystem.

The high-speed universal serial bus (USB) OTG controller is a high-speed, USB OTG dual-role-device (DRD) link controller. It supports a single USB port, which uses the ULPI interface mode, to connect to an off-chip transceiver (12-pin/8-bit data SDR mode). The high-speed USB OTG controller supports the following modes:

- USB 2.0 peripheral (function controller) in high/full speed (480/12 Mbps, respectively)

- USB 2.0 host in high/full/low speed (480/12/1.5 Mbps respectively), with one downstream port but multipoint capability when a hub is connected to it (split transaction support, etc.)
- USB 2.0 OTG DRD in high/full speed, with HNP and SRP support.

The high-speed USB host subsystem is composed of the high-speed multiport USB host controller and the USBTLL module. The high-speed multiport USB controller is a USB2.0 host controller. It contains two independent, 3-port host controllers that operate in parallel. The USBTLL module is a high-speed USB UTMI low-pin interface (ULPI) transceiverless link logic (TLL) adapter. It implements a TLL compatible with a number of USB standard interface protocols. Each USB port (1, 2, and 3) can connect either to an external-to-OMAP chip USB transceiver or directly using a transceiverless link to an external integrated circuit (IC) supporting the same TLL protocol.

For more information about the High-Speed USB OTG Controller and High-Speed USB Host Subsystem, please refer to the *Universal Serial Bus (USB)* chapter of the OMAP35x Technical Reference Manual.

20 General-Purpose I/O Interface (GPIO)

The general-purpose interface combines six general-purpose input/output (GPIO) banks.

Each GPIO module provides 32 dedicated general-purpose pins with input and output capabilities; thus, the general-purpose interface supports up to 192 (6 x 32) pins.

These pins can be configured for the following applications:

- Data input (capture)/output (drive)
- Keyboard interface with a debounce cell
- Interrupt generation in active mode upon the detection of external events. Detected events are processed by two parallel independent interrupt-generation submodules to support biprocessor operations.
- Wake-up request generation in idle mode upon the detection of external events

For more information about the GPIO modules, please refer to the *General-Purpose I/O Interface (GPIO)* chapter of the OMAP35x Technical Reference Manual.

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